CLAIMS

WHAT IS CLAIMED IS:

1. A method of manufacturing an integrated circuit, the method comprising:

providing a first gate structure and a second gate structure on a semiconductor substrate including a strained semiconductor layer, the first gate structure and the second gate structure each including a first spacer, wherein the first gate structure is provided above a first area of the strained semiconductor layer and the second gate structure is provided above a second area of the strained semiconductor layer;

providing a first masking layer above the first area;

forming first deep source and drain regions in the strained semiconductor layer in the second area;

removing the first masking layer;

masking the second area with a second masking layer;

providing a second spacer to the first gate structure; and

forming second deep source and drain regions in the strained semiconductor layer in the second area.

2. The method of claim 1, further comprising:

activating the first and second deep source and drain regions in an annealing process.

3. The method of claim 2, wherein the annealing process operates at less than 600°C.

4. The method of claim 3, wherein the removing step is a dry-etching step.

5. The method of claim 4, wherein the first and second spacers comprise nitride.

6. The method of claim 1, further comprising:

siliciding the first and second gate structures and the first and second source and drain regions.

7. The method of claim 1, wherein the first and second gate structures includes a polysilicon conductor.

8. The method of claim 1, further comprising:

covering at least a portion of the semiconductor substrate with an insulative layer.

9. The method of claim 1, wherein the second spacers are approximately 500 angstroms wide.

10. The method of claim 9, wherein the second source and drain regions include Arsenic.

11. A method of manufacturing an ultra-large scale integrated circuit including a plurality of field effect transistors having gate structures, the method comprising the steps of:

selectively providing deep source and drain regions for a first group of the field effect transistors;

selectively providing offset spacers for a second group of the field effect transistors, the second group of the field effect transistors being different than the first group of the field effect transistors, wherein the first group and the second group are provided on a top surface of a strained semiconductor layer; and

selectively providing source and drain regions for the second group.

12. The method of claim 11, further comprising:

providing a silicide layer above the source and drain regions for the first group and the second group.

13. The method of claim 12, further comprising:

providing a silicon dioxide layer over the silicide layer.

14. The method of claim 11, wherein the strained semiconductor layer includes silicon.

15. The method of claim 14, wherein the silicon is above a silicon/germanium layer.

16. The method of claim 15, wherein the offset spacers are approximately 500-2000 angstroms high and approximately 500 angstroms wide.

17. A process of forming source and drain regions on a semiconductor substrate, the process comprising:

forming a plurality of gate structures on a top surface of a strained silicon layer;

covering a first set of gate structures;

forming deep source and drain regions on each side of a second set of the gate structures;

uncovering the first set of gate structures;

covering the second set of gate structures;

providing spacers for the first set of gate structures; and

forming deep source and drain regions on each side of the first set of the gate structures.

18. The process of claim 17, further comprising:

annealing the strained silicon layer after the providing steps.

19. The process of claim 18, wherein the strained silicon layer is provided above a silicon geranium layer.

20. The process of claim 19, wherein the deep source and drain regions are provided by ion implantation.